In the outstanding Office Action, Claims 1-3 and 11 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,973,338 to Okabe (hereinafter "the '338 patent"); Claim 4 was rejected under 35 U.S.C. §103(a) as being unpatentable over the '338 patent, further in view of U.S. Patent No. 6,300,663 to Kapor (hereinafter "the '663 patent"); Claim 5 was rejected under 35 U.S.C. §103(a) as being unpatentable over the '338 patent; and Claims 6-10 were rejected under 35 U.S.C. §103(a) as being unpatentable over the '338 and '663 patents, further in view of U.S. Patent No. 6,331,466 to Takahashi et al (hereinafter "the '466 patent").

Claim 1 is directed to a power semiconductor device comprising (1) a base layer of a first conductivity type; (2) a base layer of a second conductivity type; (3) one of an emitter layer and a source layer formed on the surface of the base layer of the second conductivity type; (4) one of a collector layer and a drain layer formed on a surface of the base layer of the first conductivity type; (5) a first main electrode formed on one of the collector layer and the drain layer; (6) a second main electrode formed one of the emitter layer and the source layer and on the base layer of the second conductivity type; and (7) a gate electrode formed with first and second insulating films on the base layer of the second conductivity type that lies between one of the emitter layer and the source layer and the base layer of the first conductivity type.

The '338 patent is directed to an insulated gate type bipolar transistor (IGBT). Figure 6 of the '338 patent discloses a source electrode 61, a drain electrode 62, a gate electrode 63, a drain layer 64, a base layer 65, a source layer 66, and a drain layer 67. The Office Action identifies the drain layer 64 as "one of a collector layer and [a] drain layer" and identifies element 67 as the base layer of the first conductivity type. However, the drain layer 64 is not formed on layer 67 in the device of the '338 patent. Thus, the '338 patent does not disclose

one of a collector and a drain layer selectively formed on a surface of the base layer of the first conductivity type, as recited in Claim 1. Accordingly, Applicants respectfully traverse the rejection of Claim 1 (and dependent Claims 2 and 3) as being anticipated by the '338 patent. In addition, method Claim 11 comprises limitations analogous to those recited in Claim 1. Accordingly, Applicants respectfully traverse the rejection of Claim 11 for the reasons set forth for the patentability of Claim 1.

Regarding the rejections of Claims 4-6 under 35 U.S.C. §103(a), the Office Action relies on the '663 and '466 patents to teach the additional limitations recited in Claims 4-10. However, the Office Action also relies on the '338 patent to disclose the elements recited in Claim 1, from which Claims 4-10 depend. As discussed above, however, the '338 patent fails to disclose one of a collector layer and a drain layer selectively formed on one of the surfaces of the base layer of the first conductivity type, as recited in Claim 1. Moreover, the Office Action has not asserted that this element is taught by either the '663 or '466 patents. Thus, no matter how the teachings of the '338, '663, and '466 patents are combined, the combination does not teach a collector/drain layer formed on a surface of the base layer of the first conductivity type. Accordingly, Applicants respectfully submit that a *prima facie* case of obviousness has not been established and that the rejection of Claims 4-10 should be withdrawn.

The present amendment also sets forth new Claims 12-20 for examination on the merits. Claims 12-20, which depend from Claim 11, recite limitations analogous to the limitations recited in Claims 2-10. Thus, new Claims 12-20 are supported by the originally filed specification and do not add new matter. Moreover, Applicants submit that Claims 12-20 are patentable based on their dependence from Claim 11.

Thus, it is respectfully submitted that independent Claim 1 (and dependent Claims 2-10) and independent Claim 11 (and dependent Claims 12-20) patentably define over the cited references.

Consequently, in view of the present amendment and in light of the above discussions, the outstanding grounds of rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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1. (Amended) A power semiconductor device comprising:

a base layer of a first conductivity type;

a base layer of a second conductivity type selectively formed on one surface of said base layer of the first conductivity type;

one of an emitter layer and a source layer of the first conductivity type selectively formed on the surface of said base layer of the second conductivity type;

one of a collector layer and a drain layer selectively formed on one of the one surface and [the other] another surface of said base layer of the first conductivity type;

a first main electrode formed on said one of said collector layer and said drain layer;

a second main electrode formed on said one of said emitter layer and said source layer [of the first conductivity type] and on said base layer of the second conductivity type; and

a gate electrode formed with first and second gate insulating films on [above part of] said base layer of the second conductivity type [which] that lies between said one of said emitter layer and said source layer [of the first conductivity type] and said base layer of the first conductivity type [with first and second gate insulating films disposed therebetween;],

wherein a capacitance of a capacitor formed [of] on the second gate insulating film is different from a capacitance [that] of a capacitor formed [of] on the first gate insulating film.

2. (Amended) The power semiconductor device according to claim 1, wherein the first gate insulating film is formed in a portion near said one of said emitter layer and said source layer, [of the first conductivity type] and the second gate insulating film is formed in a portion near said base layer of the first conductivity type.

3. (Amended) The power semiconductor device according to claim 2, wherein a thickness of the second gate insulating film is larger than [that] a thickness of the first gate insulating film.

4. (Amended) The power semiconductor device according to claim 2, wherein a dielectric constant of the second gate insulating film is smaller than [that] a dielectric constant of the first gate insulating film.

5. (Amended) The power semiconductor device according to claim 2, wherein a thickness of the second gate insulating film has an inclination and the thickness thereof on a [the] side of said one of said emitter layer and said source layer [of the first conductivity type] is smaller than [that] a thickness on [the] a side of said base layer of the first conductivity type.

6. (Amended) The power semiconductor device according to claim 1, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from [the] a surface of said one of said emitter layer and said source layer [of the first conductivity type] to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

7. (Amended) The power semiconductor device according to claim 2, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from [the] a surface of said one of [the] said emitter layer and said source layer [of the first conductivity type] to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

8. (Amended) The power semiconductor device according to claim 3, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from [the] a surface of said one of [the] said emitter layer and said source layer [of the first conductivity type] to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

9. (Amended) The power semiconductor device according to claim 4, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from [the] a surface of said one of [the] said emitter layer and said source layer [of the first conductivity type] to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

10. (Amended) The power semiconductor device according to claim 5, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from [the] a surface

of said one of [the] said emitter layer and said source layer [of the first conductivity type] to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

11. (Amended) A [manufacturing] method of manufacturing a power semiconductor device comprising:

forming a base layer of a first conductivity type;

selectively forming a base layer of a second conductivity type on one surface of the base layer of the first conductivity type;

selectively forming one of an emitter layer and a source layer of the first conductivity type on a surface of the base layer of the second conductivity type;

selectively forming one of a collector layer and a drain layer on one of the one surface and [the other] another surface of the base layer of the first conductivity type;

forming a first main electrode on said one of the collector layer and the drain layer;

forming a second main electrode on said one of the emitter layer and the source layer of the first conductivity type and on the base layer of the second conductivity type; and

forming first and second gate insulating films on [on part of] the base layer of the second conductivity type [which] that lies between said one of the emitter layer and the source layer of the first conductivity type and the base layer of the first conductivity type and forming a gate electrode on the first and second gate insulating films;

wherein a capacitance of a capacitor formed on [of] the second gate insulating film is different from [that] a capacitance of a capacitor formed [of] on the first gate insulating film.

12-20. (New)